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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,030	11/24/2003	Taketo Heishi	67471-030	5444

7590 08/21/2006

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,030	HEISHI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-33* is/are allowed.

6)☒ Claim(s) *34-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/280,777.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-54 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 34-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Eickemeyer et al. (5,448,746).

3. As to claims 34,36, 40, 43,47, 48, 50, Eickemeyer taught a system that converted an instruction sequence into object codes (see conversion f source into assembly code in fig.5) including a plurality of parallel execution codes (see col.9, lines 12-35) capable of being executed by a processor in parallel comprising at least : a) an instruction scheduling unit that scheduled instructions in the instruction sequence for the parallel execution codes (see parallel and concurrent execution in col.9, lines 12-35) a bit length of the instructions and the parallel execution codes being variable wherein each of the parallel execution codes include up to N pieces of the instructions (see the instruction length code, ILC, and the two bytes for N pieces in col.12, lines 2-47) and a total bit length of each of the parallel execution codes (4 or 2 bytes) was

shorter than the sum of bit (2+4) of N pieces of the longest bit-length of the instructions;

b) instruction fetching unit (see instruction fetch in fig.5).

4. As to claims 35,44,51, Eickemeyer also included a special bit for instructing the execution of a target processor (see the scalar bit for indicating the execution of scalar processor in col.9, lines 40-60).

5. As to claims 37, 42,49, see source language in fig.5.

6. As to claims 38, 41, see the conversion of source language in fig.5

7. As to claims 39,46, 53, see instruction decoder and parallel instruction processing units in fig.5.

8. As to claim 52 , see the 4 byte boundary in col.14, lines 61-64.

9. As to claim 54, see the instruction fetching unit (see instruction fetch in fig.5).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Umekita (5,452,461) is cited for the teaching of the assignment of instructions on the instruction sequence [virtual code] to parallel codes [real code] (e.g., table , col.7, lines 50-65).

11. Claims 1-33 are allowable for the combined details of the target processor and the assignment unit (claims 1,12,18,28), the detailed fictional elements of the processor

and the opcode and the unit fields of the operand of the long instruction (claims 11,27), the combined detailed features of the register set, the decoding unit, the operation execution unit, the s+k-1 registers ,and the decoding unit (claim 24).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP